REMARKS

Applicant is in receipt of the Office Action mailed January 29, 2004.

Claims 1-28 were rejected under 35 U.S.C. 102(e) as being anticipated by Mantor et al. (U.S. Patent No. 6,624,818), hereafter referred to as Mantor.

Applicant respectfully traverses these rejections based on the following reasoning.

Claim 1 recites:

> (Original) A method for performing operations in a graphics system, wherein the graphics system includes a plurality of calculation pipelines, the method comprising:
>
> determining if a first calculation pipeline is performing a low latency operation;
>
> if the first calculation pipeline is performing a low latency operation, then providing a next operation to the first calculation pipeline; and
>
> if the first calculation pipeline is performing a high latency operation, then providing the next operation to a second calculation pipeline.

Mantor neither teaches nor suggests 1) determining if a first calculation pipeline is performing a low latency operation, 2) providing a next operation to the first calculation pipeline if the first calculation pipeline is performing a low latency operation, or 3) providing the next operation to a second calculation pipeline if the first calculation pipeline is performing a high latency operation.

Mantor does teach (col. 2, lines 61-66) a system that comprises:

> "a computation module 10 that may be used in a geometric engine of a video graphics circuit. The computation module includes a computation engine 12, an arbitration module 14, memory 16, and a plurality of thread controllers 18-24."

Mantor also teaches (col. 4, lines 9-16) that:

"The objective of the arbitration module 14 is to order the operation codes 48 such that the computation engine 12 runs at capacity (i.e. **the** pipeline within the computation engine is always full and the resources in the computation engine are efficiently utilized). Thus, for every operation cycle of the computation engine 12, the arbitration module 14 attempts to provide it with an operation code for execution."

Mantor also teaches (col. 3, lines 48-66) that:

"The arbitration module 14 receives the operation codes 38-44 from the thread controllers 18-24 and, based on an application specific prioritization scheme 46, orders the operation codes to produce ordered operation codes 48. The ordered operation codes 48 are provided to the computation engine 12 in an **ordered serial manner** for execution. The ordered operation codes 48 are provided to the computation engine at the processing rate of the computation engine 12 such that the computation engine 12 is fully utilized (i.e. **the** pipeline included in the computation engine 12 is kept full). The application specific prioritization scheme 46 is dependent on the application 26. Typically, the computation module 10 is dedicated to performing a very specific function such as processing geometric primitives for graphics processing. Since the processing of geometric primitives is very structured, the application specific prioritization scheme 46 may prioritize operations in a back-to-front manner that ensures that processing that is nearing completion is prioritized over processing that is just beginning."

Mantor also teaches (col. 3, lines 11-29) that:

"Each of the thread controllers 18-24 manages a corresponding thread and provides operation codes (op codes) 38-44 to the arbitration module 14. Each thread is a sequence of operation codes that are executed under the control of a

corresponding thread controller. Although the threads 28-34 are shown to be separate from the thread controllers 18-24, each thread may simply be a sequence of operation codes or representations of the operation codes stored within a corresponding thread controller. Each operation code includes a thread identifier that identifies the particular thread controller that issued the operation code, a type of operation to be performed, a first source address, a second source address, and a destination address. When **an** operation code is provided to the computation engine 12, the computation engine 12 executes **the** operation using data stored at the first and second source addresses and stores the result using the destination address. The source addresses and destination address may be predetermined based on the particular operation of the particular thread being executed."

Mantor also teaches (col. 3, lines 34-44) that:

"The thread controllers 18-24 each only release operation codes 38-44 when the operation codes can be executed without any potential for delay in waiting for the results of previously issued operation codes. For example, when an operation code is dependent on the results of a previously issued operation code, the thread controller will not release the dependant operation code until a certain amount of time has passed corresponding to the **latency** associated with executing the operation code that produces the data required by the dependent operation code. Preferably, each thread controller only issues one operation code at a time."

Mantor nowhere teaches or suggests a system or method for assigning an operation to one of a plurality of calculation pipelines. In fact, Mantor discusses a single pipeline within computation engine 12 and describes an **ordered serial** sequence of operations provided to the computation engine from the arbitration module 14. Furthermore, Mantor nowhere teaches or suggests a system or method for assigning an operation to one of a plurality of calculation pipelines based on the latency of a current operation being processed by the computation engine 12. In fact, the only use of the

latency of an operation is to ensure that a first operation is completed before a second operation (that depends on the results of the first) is initiated.

Therefore, claim 1 and its dependents are patentably distinguished over Mantor, for at least the reasons stated above. Claims 16, 17, and 28 recite features similar to those recited in claim 1, and thus, claim 16, claim 17 and its dependents, and claim 28 are patentably distinguished over Mantor based on reasoning similar to that given above in support of claim 1.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5181-87600/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

Respectfully submitted,

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